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# Substantial reduction of the dielectric losses of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films using a $SiO_2$ barrier layer

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**Abstract**

The efficient use of ferroelectric thin films in radio-frequency agile devices faces several limitations. One of them is imposed by the dielectric losses which are usually above 1%, i.e. above the threshold as set by the electronic industry. Following the same route as for bulk ceramics, we have processed composite stacks made of BST/$SiO_2$ multilayers using radio-frequency magnetron sputtering. Doing so, we were able to repeatedly achieve dielectric losses well below 0.5% while keeping a high dielectric susceptibility and a suitable tunability. All of these improvements have been observed at low frequencies ($f < 10$ MHz) and the transfer to the targeted frequency range ($f > 1$ GHz) is currently in progress.

## 1. Introduction

Ferroelectric thin films are good candidates for use in the processing of agile devices such as filters, phase shifters and antennas [1–3]. This is because their high dielectric susceptibility can easily be tuned by a dc electric bias. The thin films most studied for this purpose are within the solid solution $BaTiO_3$–$SrTiO_3$ group and the optimal composition is the so-called 60/40 one ($Ba_{0.6}Sr_{0.4}TiO_3$—BST in the following), whose ferroelectric phase transition is slightly below room temperature [4].

Even before thinking of any integrated device, there are however several drawbacks imposed by these BST films themselves, the most difficult to overcome arising from the dielectric losses. Indeed, intrinsic dielectric losses in BST films are observed starting from low frequencies and increasing when reaching the targeted frequency range ($f > 1$ GHz). Many sources have been proposed for these losses including point defects, grain boundaries, interfaces between the films and their electrodes [5–8]. We note that such losses are also observed in single crystals and bulk ceramics [9] which suggests a possible intrinsic and thus unavoidable origin for the dielectric losses. In ceramics, the composite route has been used from the beginning of the 1990s to overcome such drawbacks [10]. The idea was to add to the ferroelectric BST grains a dielectric phase with very low dielectric losses. Such dielectric

  

barriers in the high frequency range were selected within already existing materials: MgO, $MgTiO_3$, . . .. Recently, the coating of individual BST grains by a $SiO_2$ shell has been proposed to achieve a better control of the ceramic architecture and thus of its dielectric parameters [11]. In the context of thin films, the favourable effect of doping with acceptor cations on the leakage current of BST films has been extensively studied [12–14], but the stability of such films is not evident. A thin homo-buffer layer of BST having a different composition from the main BST layer has also been used to decrease the losses [15]. But this buffer layer is not single phased, which complicates the reproducibility of the process.

Starting with the same idea as for bulk ceramics, the composite route has already been taken to reduce the dielectric losses of BST [16]. Multilayers of BST alternated with MgO dielectric barriers have also been deposited by the sol–gel technique, but diffusion of the low loss phase in the BST matrix occurred upon annealing [17]. Moreover, the direct influence of this stacking on the dielectric parameters has not been quantified up to now. In this paper, we follow the trend which has been initiated in our laboratory recently of using silicon oxide as a coating agent for BST individual grains. We transfer this core–shell concept to integrated devices with a stacking of $SiO_2$/BST layers with the main aim of decreasing the BST losses due to the $SiO_2$ dielectric barrier. $SiO_2$ does indeed have extremely low losses up to high frequencies and is very stable chemically. We show here that, in the low frequency range, this has been achieved and that the dielectric susceptibility and the tunability have been kept within a useful range.

## 2. Experimental details

The films and multilayers have been processed using a four-target magnetron sputtering station which allows the stacks to be deposited without breaking off from the process. This station is equipped with *in situ* optical spectroscopy and mass spectroscopy for continuously checking the plasma stability. The base pressure was lower than $2 \times 10^{-5}$ Pa and the argon overpressure was 5 Pa for the sputtering of both the BST and the $SiO_2$ films. Si(100) and Pt(111)/$TiO_2$/$SiO_2$/Si (denoted as Pt/Si subsequently) substrates were kept at 600 or 700 °C throughout the whole process. All these parameters have been previously optimized for $BaTiO_3$ derived films [18] and slightly tuned for the deposition of $SiO_2$ films. For BST layers, a ceramic target of density higher than 90% and diameter 51 mm was processed in our laboratory. For $SiO_2$ layers, we used a silicon commercial target of 51 mm diameter. This explains why the main parameter which was changed as compared to the BST films case is the partial pressure of oxygen, which was higher for $SiO_2$ (5% as compared to 1%). Two types of architecture were prepared: BST/$SiO_2$ bilayers and BST/$SiO_2$/BST trilayers, in order to determine the influence of the position of the dielectric layer in the stack on its electrical properties. Monolayers of BST and of $SiO_2$ were also prepared in the same conditions, as references.

Since our aim is to keep the dielectric properties (permittivity and tunability) as close as possible to those of individual BST layers, the $SiO_2$ layer must be much thinner (at least ten times) than the BST one. Hence, for each type of architecture the $SiO_2$ thickness was changed from 5 to 35 nm, keeping the BST thickness close to 300 nm. The $SiO_2$/BST thickness ratio was thus swept from approximately 1.5% to 12%.

To probe the dielectric parameters of the stacks, platinum dots were sputtered in the same chamber through 250 $\mu$m holes made in a stainless steel mask. The samples with top electrodes were post-treated by rapid thermal annealing (RTA) at 600 °C for 1 min in air in order to improve the interface between the top Pt and the dielectric stack.

The top and bottom platinum electrodes were connected to an HP4194 impedance analyser through a two-tip Karl Süss sample holder and four BNC wires. The operating frequency was

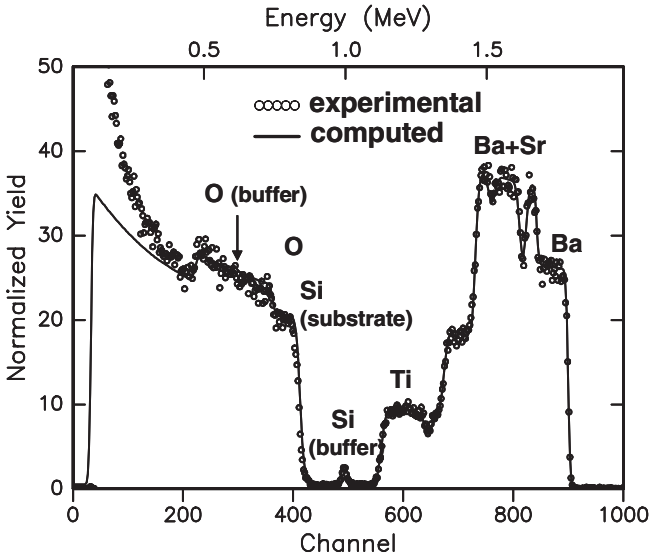


**Figure 1.** RBS data and their simulation for a BST(150 nm)/$SiO_2$(11 nm)/BST(150 nm)/Si stack deposited at 600 °C under 5 Pa.

swept from 100 Hz to a 15 MHz with an ac probing signal of 500 mV. For tunability experiments, the internal bias could be swept between −40 and 40 V. Due to the electrical connections, the useful frequency range was limited to 1 MHz. The tunability, corresponding to the decrease of $\varepsilon'$ with the applied field $E$, is expressed as $T = |[\varepsilon'(E) - \varepsilon'(E = 0)]|/\varepsilon'(E = 0)$. All the values given subsequently were computed at 100 kHz and 800 kV cm$^{-1}$. The dielectric experiment was computer controlled using home-made software. All the data reported here stem from the averaging over 12 capacitors for a given stack. The out-of-plane structure of the films was analysed using standard $\theta$–$2\theta$ x-ray diffraction. The chemical profiling of Ba, Sr, Ti for BST films was achieved using Rutherford backscattering spectroscopy (RBS) on the films deposited on Si(100). A $He^+$ beam of 2 MeV is focused on the films, and spectrometry as regards the energy of the backscattered ions allows a chemical analysis and a thickness computation (assuming a 100% density of the film). The individual thicknesses of $SiO_2$ layers in the stacks were determined by contact profilometry, measuring the deposition rate from $SiO_2$ monolayers and assuming the same rate for the stacks. It was also directly confirmed by RBS simulation and SEM observation.

## 3. Results and discussion

The chemical content and the thicknesses of individual layers in the stacks were probed by RBS. The Pt bottom layer prevents chemical analysis for on Pt/Si substrates, because the energy peak of strontium overlaps with that of platinum. Films on silicon were then probed after deposition in the same conditions as those on platinized substrates.

Figure 1 shows RBS data and their simulation for a BST(150 nm)/$SiO_2$(11 nm)/BST(150 nm)/Si stack. The simulation gives the following composition for the BST layers: Ba 0.55/Sr 0.41/Ti 1.04, which corresponds to a (Ba + Sr)/Ti ratio of 0.92. The stoichiometry of the ceramic target is not fully retained during the growth of the films by rf magnetron sputtering.

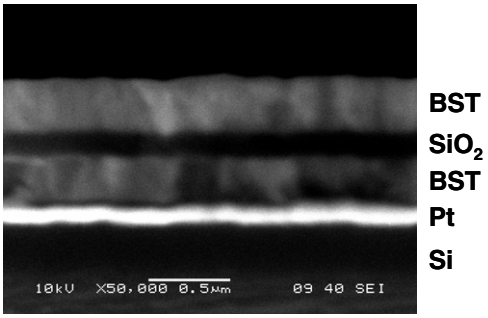


**Figure 2.** An SEM micrograph a BST(300 nm)/$SiO_2$(150 nm)/BST(300 nm)/Pt/Si multilayer deposited at 600 °C.

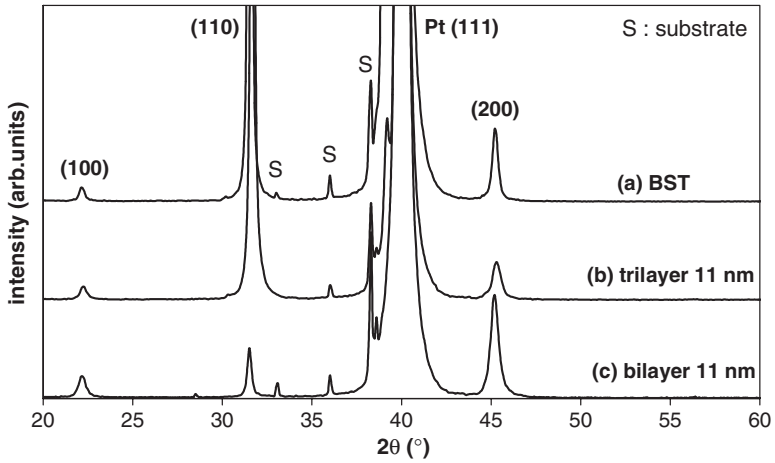


**Figure 3.** XRD patterns for $BST_6$/Pt/Si (a), $BST_6/SiO_2/BST_6$/Pt/Si (b) and $BST_6/SiO_2$/Pt/Si (c) stack deposited at 600 °C, with 11 nm $SiO_2$ thickness for the multilayers.

RBS data also confirm the thicknesses obtained by contact profilometry. The same analyses were performed on BST films and on all our stacks, and confirmed that the BST layer always kept a composition close to 60/40.

SEM observations on multilayers with thicker $SiO_2$ layers (see figure 2) confirmed that the $SiO_2$/BST interface is sharp and that the mechanical stability of the stack is of high quality. This was already checked for $BaTiO_3$ films on amorphous $SiO_2$ substrates [19] and for the coating of $SiO_2$ nanosize layers on BST grains [11].

Figure 3 compares the x-ray diffraction patterns of a bilayer (c) and a trilayer (b) on Pt(111)/$TiO_2$/$SiO_2$/Si substrates with a BST reference (a). All the films are polycrystalline and show the (100), (110) and (200) perovskite peaks of the BST phase. The BST layers alone display a powder pattern with a strong ($hh$0) preferential orientation. Note that the BST(111) diffraction peak is not resolved from the very intense Pt(111) peak.

As long as a thin layer of $SiO_2$ is deposited on Pt/Si substrate prior to the BST deposition (figure 3(c)), this ($hh$0) preferential orientation is completely relaxed, whatever the $SiO_2$ thickness (in the range studied). Moreover, in all cases, no diffraction lines coming from the $SiO_2$ buffer layer could be observed, confirming its amorphous nature. This buffer layer is thus a barrier to the preferential orientation of the BST layer. Similar structural evolution

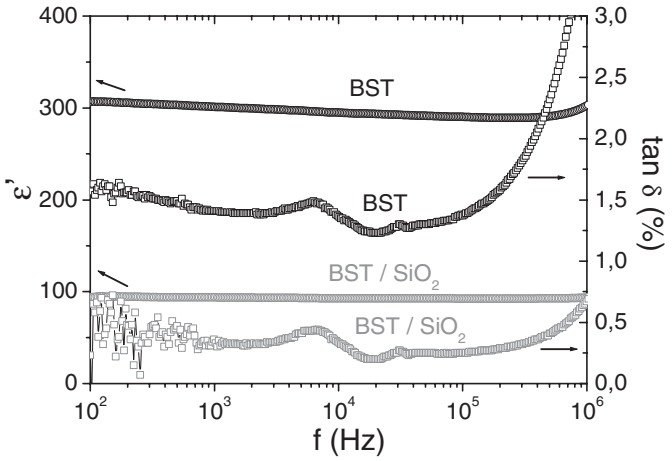


**Figure 4.** The frequency dependence of the permittivity and dielectric losses of a BST (330 nm) monolayer and a BST(330 nm)/$SiO_2$(11 nm) bilayer deposited at 600 °C on platinized silicon.

of the stack occurred on (100) silicon: the $SiO_2$ layer prevented the slight (100) preferential orientation of the BST layer, due to the (100) orientation of the substrate in this case.

When the $SiO_2$ layer is deposited between two BST layers, the XRD patterns are very different (figure 3(b)). In this case, the strong (*hh*0) preferential orientation is only very slightly altered by the $SiO_2$ layer, and the contributions of each of the BST layers cannot be differentiated.

XRD patterns for BST/Si(100) films and BST/$SiO_2$/Si(100) bilayers at 600 and 700 °C substrate temperatures were fully analysed. For both types of sample, increasing the deposition temperature from 600 to 700 °C results in a strong (100) preferential orientation, whatever the $SiO_2$ thickness for the bilayers. Moreover, it also results in a decrease of the FWHM for all perovskite peaks, and in a decrease of the cell parameter (4.023 Å at 600 °C and 3.992 Å at 700 °C, for monolayers and bilayers, compared to 3.965 Å for bulk BST). Increasing the deposition temperature thus allows a better crystallinity, the $SiO_2$ layer playing no important role for bilayers on Si(100).

Preliminary experiments allowed us to prepare BST monolayers stacked between two platinum electrodes, with permittivities around 300 and dielectric losses of 1.4%. The very useful property of such material in thin film is that its dielectric susceptibility is decreased by more than about 50% under a dc field of 800 kV $cm^{-1}$. Figure 4 compares the dielectric properties of a BST monolayer with those of a BST/$SiO_2$ bilayer, showing that the insertion of a $SiO_2$ barrier layer allows a strong decrease of the dielectric losses: at 100 kHz, they are reduced from 1.4 to 0.3% thanks to a 11 nm thick $SiO_2$ film. The permittivity of silica being much lower than that of BST, its impact on the permittivity of the stack is obviously negative, but such a bilayer still presents a permittivity of about 100.

Figure 5 shows the electric field dependence of BST and BST/$SiO_2$/Pt/Si stacks with different $SiO_2$ layer thicknesses, keeping the BST thickness constant (330 nm). The impact of the buffer layer on the dielectric losses is confirmed: of greatest interest is the strong decrease thanks to this barrier, well below 0.5% and even towards 0.1%. Moreover, the stacks with $SiO_2$ no longer exhibit an electric field dependence of the losses. Such a dielectric barrier could also be efficient in the GHz frequency range, thus decreasing the intrinsic dielectric losses of BST in this frequency range. Further experiments, including the in-plane design of metallic electrodes is needed, in order to confirm this point.

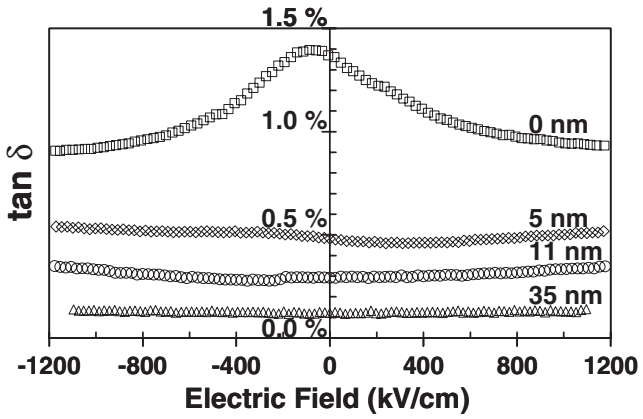


**Figure 5.** The electric field dependence of the dielectric losses at 100 kHz for BST and BST/$SiO_2$ bilayers with different $SiO_2$ layer thicknesses.

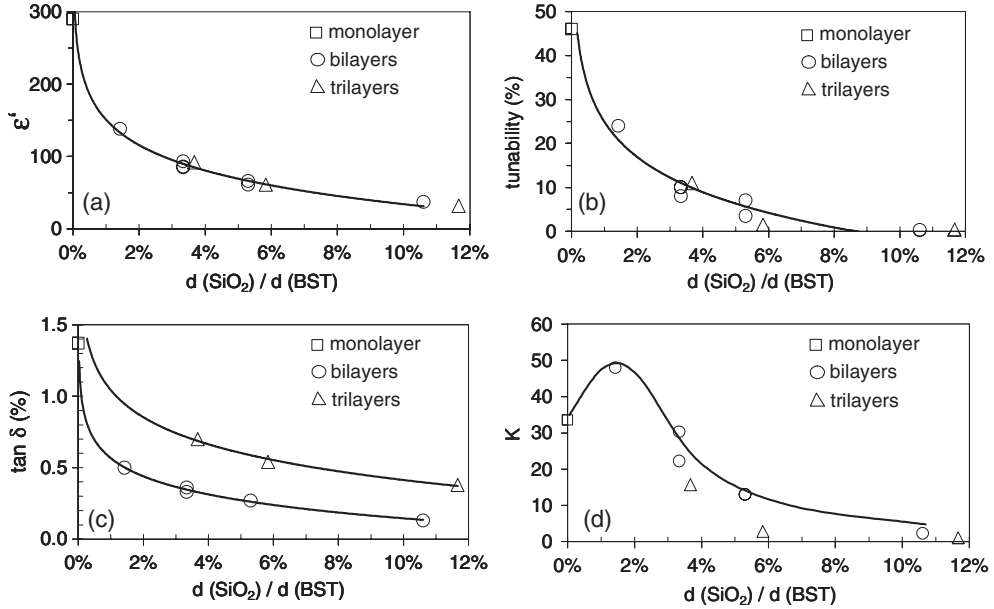


**Figure 6.** Evolution of the dielectric properties at 100 kHz of BST/$SiO_2$ multilayers deposited at 600 °C with the $SiO_2$/BST thickness ratio ((a) permittivity, (b) tunability under 800 kV $cm^{-1}$, (c) dielectric losses, (d) figure of merit under 800 kV $cm^{-1}$).

The $SiO_2$ thickness dependences of the dielectric properties at 100 kHz of bilayers and trilayers, compared to a BST reference, are shown in figures 6(a)–(d). When the thickness $d(SiO_2)$ of the $SiO_2$ buffer layer increases, the effective dielectric susceptibility decreases as expected. This decrease is independent on the position of the $SiO_2$ layer: the susceptibilities are the same for bilayers and trilayers having the same $d(SiO_2)/d(BST)$ ratio. The permittivity of our multilayers has been computed, assuming a perfect series association of capacitors, and setting values of 4 for $SiO_2$ and 300 for BST. The measured permittivities are then almost identical to the computed ones: the BST and $SiO_2$ layers in the stacks exhibit the expected permittivity values.

The same behaviour as for the permittivity is observed for the tunability (figure 6(b)), which is greatly reduced by the addition of a dielectric barrier, the electric field being mainly applied to the lowest capacitance, i.e. the $SiO_2$ non-tunable layer.

Contrary to the previous properties, the evolution of the losses depends on the position of the $SiO_2$ layer in the stack (figure 6(c)): trilayers exhibit higher losses than bilayers with the same $d(SiO_2)/d(BST)$. The number of BST/$SiO_2$ interfaces seems thus to play a role in the losses. Moreover, the texturizing of trilayers (cf figure 3) could imply a higher roughness and thus a not so good interface quality. Deposition of stacks with more layers and atomic force microscopy investigations are currently in progress in order to confirm these observations.

A figure of merit $K$ can be used to describe the quality of our multilayers. $K$ is defined as the ratio of the tunability for a given applied dc field to the dielectric losses under no bias. Figure 6(d) shows that this $K$ factor reaches a maximum value of almost 50 for a 5 nm thick $SiO_2$ buffer layer under the BST film. For technological application, another compromise can be reached between a high permittivity and low losses. In this way, a bilayer with 3% thickness $SiO_2$ under a BST layer gives an optimized stack with a permittivity of 100, dielectric losses as low as 0.3% (and independent of the applied electric field) and a tunability of 10% at 800 kV $cm^{-1}$.

First dielectric measurements on multilayers deposited on platinized silicon at 700 °C show the same trend, the permittivity and tunability but also the losses being higher than for films deposited at 600 °C. This is consistent with the better crystallinity already observed at 700 °C, the increase of the losses being explained by the higher roughness (forthcoming AFM measurements).

## 4. Conclusion

We have demonstrated that the use of an amorphous $SiO_2$ buffer layer combined with the well-known BST allows one to decrease the dielectric losses of the stacks well below 0.5% and even towards 0.1%, controlling the thicknesses ratio of both materials. The $SiO_2$ thickness dependence of the dielectric properties for the stacks was studied in detail and showed that this improvement of the losses can be achieved while keeping acceptable values for the permittivity and tunability. Considering a figure of merit based on the tunability and losses, optimized properties are obtained for a 5 nm thick $SiO_2$ layer grown prior to the BST (330 nm) film. All these improved parameters have to be confirmed in the actual operating frequency range ($f > 1$ GHz) which needs further experimental work.

This new and very simple way of using layered structures to control the losses of BST-based capacitors for applications to high frequency devices is perfectly compatible with the semiconductor industry.

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